COURSE CODE: 20EC0402 **R20**

SIDDHARTH INSTITUTE OF ENGINEERING & TECHNOLOGY:: PUTTUR

(AUTONOMOUS)

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QUESTION BANK (DESCRIPTIVE)

Subject with Code: Electronic Devices and Circuits(20EC0402)

Course & Branch: B.Tech.–ECE

Regulation: R20 **Year & Sem:** II-B.Tech.& I-Sem.

UNIT –I
PN JUNCTION DIODE

1	a)	Describe the construction of PN Junction Diode.	[L1][CO1]	**[3M]**
	b)	Define the terms a) Doping b) Depletion region c) Barrier Potential	[L1][CO1]	**[3M]**
	c)	Illustrate the working of a PN Junction diode under forward bias and reverse bias with neat schematic diagrams	[L1][CO1]	**[4M]**
	d)	Sketch the V-I Characteristics of a PN Junction Diode.	[L2][CO3]	**[2M]**
2	a)	Define Break down voltage and cut in voltage and give the typical values of cut-in voltage for Si and Ge diodes.	[L1][CO3]	**[2M]**
	b)	Analyze the current components of a PN Junction Diode and derive the diode current equation.	[L4][CO2]	**[6M]**
	c)	When a reverse bias is applied to a germanium PN Junction Diode, the reverse saturation current at room temperature is 0.3μA. Determine the current flowing in the diode when 0.15V forward bias is applied at room temperature.	[L3][CO3]	**[4M]**
3	a)	Discuss the effect of temperature on V-I characteristics of a PN Junction Diode.	[L2][CO3]	**[5M]**
	b)	The reverse saturation current of a silicon PN Junction Diode is 10μA. Calculate the diode current for the forward bias voltage of 0.6V at 25^0C.	[L3][CO3]	**[4M]**
	c)	Draw the ideal diode characteristics of PN Junction Diode and give its circuit symbol.	[L1][CO3]	**[3M]**
4	a)	A PN junction germanium diode has a reverse saturation current of 10 μA at the room temperature of 27^0C. It is observed to be 30μA, when the room temperature is increased. Calculate the new room temperature.	[L3][CO2]	**[6M]**
	b)	Discuss about the forward and reverse resistances of a PN junction diode.	[L2][CO3]	**[6M]**
5	a)	Derive the expression for forward dynamic resistance of a PN junction diode.	[L3][CO2]	**[7M]**
	b)	Calculate the forward resistance of a PN Junction Diode when the forward current is 5mA at T = 300 K. Assume Silicon diode.	[L4][CO2]	**[5M]**
6	a)	What is diode capacitance? Mention its types.	[L1][CO1]	**[2M]**

	b)	Define Transition and Diffusion capacitances of a PN Junction Diode.	[L1][CO3]	**[4M]**
	c)	Derive the expression for transition capacitance of a PN Junction Diode.	[L3][CO2]	**[6M]**
7	a)	Derive the expression for Diffusion capacitance of a PN Junction Diode.	[L3][CO3]	**[8M]**
	b)	List the applications of PN Junction.	[L1][CO1]	**[4M]**
8	a)	Explain Breakdown mechanisms in PN Junction Diode.	[L2][CO3]	**[6M]**
	b)	Draw the circuit symbol of Zener diode and label its terminals.	[L1][CO1]	**[2M]**
	c)	Sketch and explain the V-I characteristics of Zener Diode and mention its application.	[L3][CO3]	**[4M]**
9	a)	Show that the Zener Diode can act as a voltage regulator with a neat circuit diagram.	[L2][CO4]	**[4M]**
	b)	Define clippers and Clampers. Also list their types.	[L1][CO1]	**[2M]**
	c)	Explain about a Combination Clipper and sketch its input – output waveforms.	[L2][CO4]	**[4M]**
	d)	Mention the applications of Zener diode.	[L1][CO1]	**[2M]**
10	a)	Construct the Positive and Negative Diode Clippers and explain with neat waveforms.	[L3][CO4]	**[4M]**
	b)	What is a Clamper circuit? Describe about positive and negative clampers with neat circuit diagram.	[L1][CO4]	**[4M]**
	c)	Design a Biased positive series clipper to clip the sinusoidal voltage waveform at +2 volts. The sinusoidal waveform has peak to peak amplitude of 10 volts.	[L3][CO6]	**[2M]**

UNIT –II
RECTIFIERS, FILTERS AND SPECIAL PURPOSE DEVICES

1.	a)	Define a Rectifier and list its types.	[L1][CO1]	**[2M]**
	b)	Draw the circuit diagram of a Half Wave Rectifier and explain its operation with the help of waveforms.	[L1][CO4]	**[3M]**
	c)	Define the following terms: i) Ripple factor ii) Efficiency iii) Peak inverse voltage iv) Transformer utilization factor	[L1][CO2]	**[3M]**
	d)	Derive the expressions for Average DC Voltage, RMS Value of voltage, DC Output Power and AC input Power for a Half Wave Rectifier.	[L3][CO5]	**[4M]**
2.	a)	Draw the circuit diagram of a Full Wave Rectifier and with the help of waveforms describe its operation.	[L1][CO4]	**[6M]**
	b)	Derive the expressions for Average DC current, RMS Value of Current, DC Power Output and AC Power input for a Full Wave Rectifier. List the advantages.	[L3][CO5]	**[4M]**
	c)	List the advantages and disadvantages of FWR and HWR.	[L1][CO1]	**[2M]**
3.	a)	A Half Wave Rectifier is supplied from a 230V, 50 Hz supply with a step-down ratio of 3:1 to a resistive load of 10kΩ. The diode forward resistance is 75Ω while transformer secondary is 10Ω. Calculate maximum, average, RMS values of current, DC output voltage, efficiency of rectification and ripple factor.	[L4][CO5]	**[6M]**
	b)	A Full Wave Rectifier circuit is fed from a transformer having a center-tapped secondary winding. The RMS voltage from either end of secondary to center tap is 30V. If the diode forward resistance is 2Ω and that of the half secondary is 8Ω, for a load of 1 KΩ. Calculate DC power delivered to the load, efficiency of rectification and Transformer Utilization Factor (TUF) of secondary.	[L4][CO5]	**[6M]**
4.	a)	With a neat circuit diagram and waveforms, illustrate the working of a Bridge rectifier.	[L2][CO3]	**[4M]**
	b)	A 5KΩ load is fed from a bridge rectifier connected across a transformer secondary whose primary is connected to 460V, 50 Hz supply. The ratio of number of primary turns to secondary turns is 2:1. Estimate DC load current, ripple voltage and PIV rating of diode.	[L4][CO5]	**[4M]**
	c)	Compare different rectifiers.	[L2][CO2]	**[4M]**
5.	a)	Define a filter and give its types.	[L2][CO1]	**[2M]**
	b)	Draw the circuit diagram of Full Wave Rectifier with Inductor filter and illustrate its operation. Also derive the expression for ripple factor.	[L3][CO3]	**[5M]**

	c)	Find the value of inductance to be used in the Inductor filter connected to a Full Wave Rectifier operating at 60 Hz to provide a DC output with 4% ripple for a 100Ω load.	[L3][CO6]	**[3M]**
	d)	List the advantages and disadvantages of FWR with inductor Filter.	[L1][CO5]	**[2M]**
6.	a)	With neat circuit diagram and waveforms, explain the operation of Full Wave Rectifier with Capacitor filter and derive the expression for its ripple factor.	[L3][CO3]	**[6M]**
	b)	Calculate the value of capacitance to be used in a Capacitor filter connected to a full wave rectifier operating at a standard aircraft power frequency of 400 Hz, if the ripple factor is 10% for a load of 500Ω.	[L4][CO6]	**[3M]**
	c)	List the advantages and disadvantages of FWR with capacitor filter.	[L1][CO5]	**[3M]**
7.	a)	Demonstrate the working principle of LC filter with neat circuit diagram and derive the expression for its ripple factor. List its advantages and disadvantages.	[L4][CO3]	**[5M]**
	b)	Explain the working principle of CLC or π section filter and derive expression for its ripple factor.List its advantages and disadvantages.	[L4][CO3]	**[5M]**
	c)	Compare different rectifiers with filter circuits.	[L2][CO2]	**[2M]**
8.	a)	Draw the circuit symbol of Varactor diode, give its characteristics. and list its applications.	[L1][CO1]	**[6M]**
	b)	Draw the circuit symbol of Tunnel diode. Explain the Volt-Ampere (V-I) characteristics with the help of energy band diagrams and List its applications.	[L2][CO3]	**[6M]**
9.	a)	Draw the circuit symbol of UJT and its characteristics with neat diagram and list its applications.	[L1][CO1]	**[6M]**
	b)	Explain the construction, working and applications of Solar Cell.	[L2][CO3]	**[6M]**
10.	a)	Give the classification of LCD based on construction and explain. List the advantages and applications of LCD.	[L2][CO1]	**[6M]**
	b)	With neat diagram, explain the working of LED and list its advantages and applications.	[L3][CO3]	**[6M]**

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UNIT –III
TRANSISTOR CHARACTERISTICS: BJT & FET

1	a)	Define a transistor. Draw the circuit symbols of PNP and NPN transistor and label all terminals.	[L1][CO1]	**[2M]**
	b)	Explain the construction of NPN transistor with a neat diagram.	[L2][CO1]	**[5M]**
	c)	If the base current in a transistor is 20µA when the emitter current is 6.4mA, what are the values of α and β? Also calculate the collector current.	[L2][CO2]	**[5M]**
2	a)	Explain the operation of NPN transistor.	[L2][CO3]	**[6M]**
	b)	Explain the current components of a PNP transistor.	[L2][CO3]	**[6M]**
3	a)	Evaluate the relation between α and β of a Transistor.	[L3][CO2]	**[5M]**
	b)	With a neat diagram, explain how a transistor acts as an amplifier.	[L1][CO3]	**[7M]**
4	a)	With neat diagram, explain the Input and Output characteristics of a BJT in CB Configuration. Explain Early effect.	[L2][CO3]	**[5M]**
	b)	Define the following terms: i) Emitter efficiency ii) Transport factor iii) Large signal current gain	[L1][CO2]	**[3M]**
	c)	For a transistor, the leakage current is 0.1µA in CB configuration, while it is 19µA in CE configuration. Find α & β of the transistor?	[L2][CO2]	**[4M]**
5	a)	Explain the Input and Output characteristics of a BJT in CE Configuration.	[L2][CO3]	**[4M]**
	b)	Why CE configuration is most widely used in amplifier circuits?	[L4][CO5]	**[2M]**
	c)	Illustrate the Input and Output characteristics of BJT in CC Configuration.	[L2][CO3]	**[3M]**
	d)	Compare Transistor configurations.	[L4][CO2]	**[3M]**
6	a)	Define FET and explain different types of FET.	[L2][CO1]	**[5M]**
	b)	Explain the construction and working principle of N-Channel JFET.	[L2][CO3]	**[7M]**
7	a)	Explain the characteristics of N-Channel JFET and define JFET parameters.	[L2][CO3]	**[5M]**
	b)	Explain the construction and Characteristics of N-Channel depletion type MOSFET.	[L2][CO1]	**[7M]**
8	a)	Draw the circuit symbols of different JFETs and MOSFETs and list their applications.	[L2][CO3]	**[2M]**
	b)	With the help of neat diagram, explain the construction and operation of N-channel enhancement type MOSFET.	[L1][CO2]	**[4M]**
	c)	Compare BJT with JFET.	[L4][CO2]	**[4M]**
9	a)	List the differences between Depletion and Enhancement MOSFETs.	[L2][CO2]	**[6M]**
	b)	Explain the operation of N-Channel depletion type MOSFET with diagram.	[L2][CO3]	**[6M]**
10	a)	Explain the characteristics of N-Channel enhancement type MOSFET.	[L2][CO1]	**[6M]**
	b)	Compare the performance of JFET with MOSFET.	[L1][CO1]	**[6M]**

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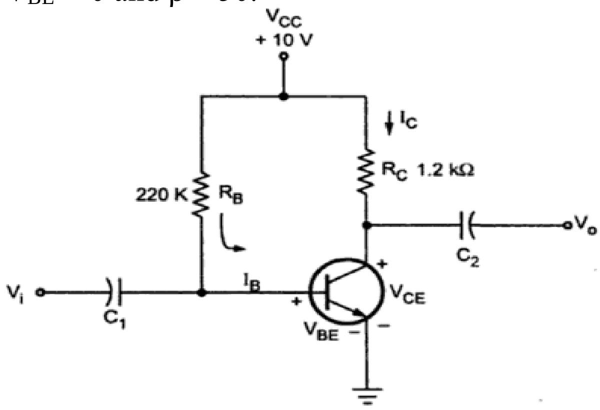
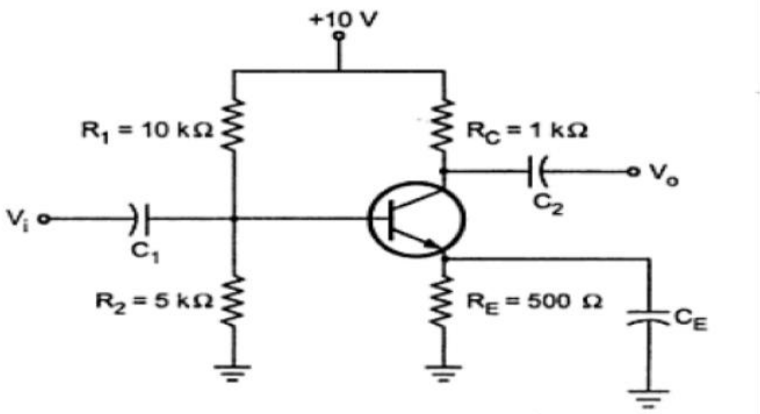
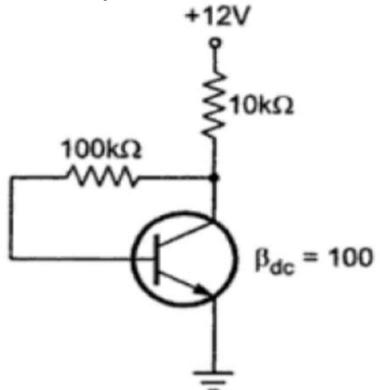
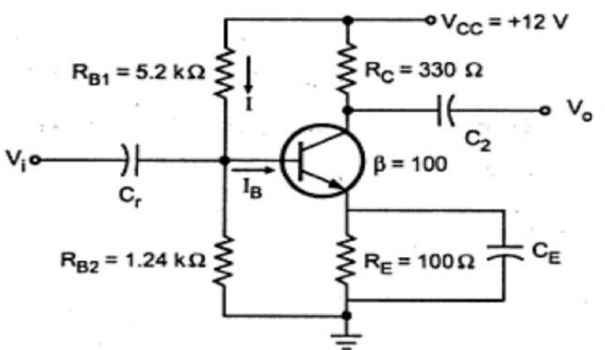
UNIT- IV
TRANSISTOR BIASING AND THERMAL STABILIZATION

1	a)	Define transistor biasing and explain the need for biasing.	[L1][CO2]	**[3M]**
	b)	Derive the expression for Stability Factor, $S_{f.}$ from Collector current equation.	[L4][CO3]	**[4M]**
	c)	Explain the concept of DC and AC Load lines and discuss the criteria for fixing the Q-point.	[L2][CO3]	**[5M]**
2	a)	List the different types of Biasing a Transistor and explain the Fixed Bias of a Transistor.	[L2][CO3]	**[7M]**
	b)	Determine the expression for stability factor, S for fixed bias circuit and list its disadvantages.	[L3][CO5]	**[5M]**
3	a)	Explain Collector to Base bias of a Transistor with neat circuit diagram and determine Q-point.	[L2][CO5]	**[6M]**
	b)	For the circuit shown in the Figure, solve I_B, I_C, V_{CE}, V_B , V_C and V_{BC}. Assume that V_{BE} = 0 and β = 50. 	[L3][CO5]	**[6M]**
4	a)	Define Stability Factor, S. Derive the stability factor, S for collector to base bias of BJT.	[L3][CO5]	**[6M]**
	b)	Design a collector to base bias circuit for the specified conditions: V_{cc} = 15V, V_{CE} = 5V, I_C = 5mA and β = 100.	[L3][CO6]	**[6M]**
5	a)	Draw the circuit diagram of Self Bias of a Transistor and determine its Q-point.	[L3][CO6]	**[6M]**
	b)	Estimate the stability factors S, S' and S'' of a BJT Voltage Divider bias.	[L3][CO5]	**[6M]**
6	a)	Define Bias compensation technique and mention its types.	[L1][CO3]	**[4M]**
	b)	Explain Diode Compensation Technique for the parameters of V_{BE} and I_{CO}.	[L2][CO4]	**[6M]**
7	a)	Illustrate Thermistor Compensation Technique for stabilization against variations in Q-point.	[L2][CO4]	**[6M]**

	b)	For the circuit shown in Figure, β = 100 for the silicon transistor. Calculate V_{CE} and I_C. 	[L3][CO6]	**[6M]**
8	a)	Define and Explain Thermal Runaway and Thermal Resistance.	[L2][CO2]	**[6M]**
	b)	Determine the Q-point for the circuit shown in the Figure 	[L3][CO6]	**[6M]**
9	a)	Draw the DC load line for the following transistor configuration. Obtain the quiescent point. 	[L3][CO6]	**[6 M]**
	b)	Calculate the values of Resistors in a fixed bias circuit using the following specifications: I_{CQ}=9.2mA, V_{CEQ}=4.4.v, h_{fe}=1115, V_{BE}=0.7v & V_{CC}=9v.	[L3][CO6]	**[6M]**
10	a)	Estimate the condition for achieving Thermal Stability.	[L2][CO4]	**[6M]**
	b)	If the various parameters of a CE amplifier which uses the self bias method are V_{CC}=12v, R_1=10KΩ,R_2=5KΩ,R_c=1KΩ, R_E=2KΩ & β=100, find the operating point. Assume Si Transistor.	[L3][CO6]	**[6M]**

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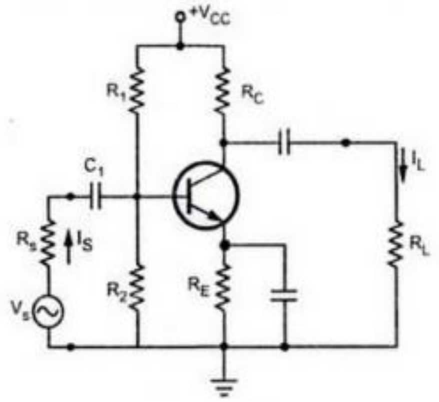
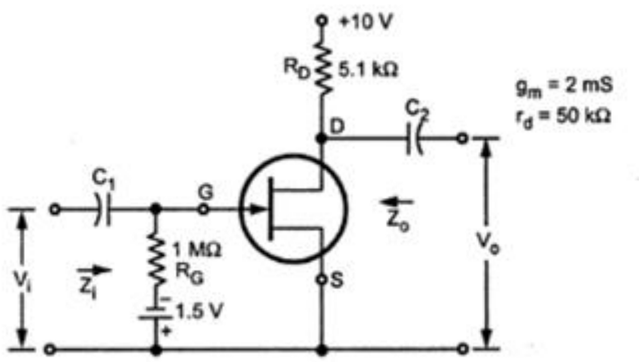
UNIT- V
SMALL SIGNAL LOW FREQUENCY TRANSISTOR AMPLIFIER

1	a)	What is a small signal low frequency transistor amplifier?	[L1][CO2]	**[2M]**
	b)	Define h-parameters and draw the generalized h-parameter model of a Transistor. Why hybrid model is used for the analysis of BJT amplifier at low frequencies?	[L2][CO2]	**[4M]**
	c)	Draw the hybrid model for a transistor in CE configuration and derive its hybrid parameters.	[L2][CO2]	**[6M]**
2	a)	Using low frequency h-parameter model, evaluate the expressions for voltage gain, current gain, input impedance and output admittance for a BJT Amplifier in CE configuration.	[L2][CO4]	**[7M]**
	b)	A CE amplifier is driven by a voltage source of internal resistance R_s = 800Ω and the load impedance of R_L=1000Ω. The h-parameters are h_{ie}=1k, h_{fe}=50, h_{oe} = 25μA/V and h_{re} = 2 x 10^{-4}. Find current gain, voltage gain, input impedance and output impedance using exact analysis.	[L3][CO5]	**[5M]**
3	a)	With neat diagram, summarize the parameters of CE amplifier using approximate analysis.	[L2][CO5]	**[6M]**
	b)	Examine the expressions for current gain, voltage gain, input impedance and output impedance of CB amplifier using simplified hybrid model.	[L2][CO5]	**[6M]**
4	a)	Draw the simplified h-parameter model for a transistor in CE, CB and CC configuration.	[L1][CO2]	**[6M]**
	b)	A CE amplifier is driven by a voltage source of internal resistance R_s = 800Ω and the load impedance of R_L=1000Ω. The h-parameters are h_{ie}=1k, h_{fe}=50, h_{oe} = 25μA/V and h_{re} = 2 x 10^{-4}. Find current gain, voltage gain, input impedance and output impedance using approximate analysis.	[L3][CO5]	**[6M]**
5	a)	Derive expressions for Ai, R_i, A_v and R_0 for a Common Collector Amplifier using simplified hybrid model.	[L3][CO5]	**[6M]**
	b)	A voltage source of internal resistance, R_s = 900Ω drives a CC amplifier using load resistance R_L=2000Ω. The CE h parameters are h_{fe}=60, h_{ie}=1200Ω, h_{oe} = 25μA/V and h_{re} = 2 x 10^{-4}. Calculate A_I, R_i, A_v and R_0 using approximate analysis.	[L4][CO5]	**[6M]**
6	a)	For a CB transistor, amplifier driven by a voltage source of internal resistance R_s = 1200Ω, the load Impedance of R_L = 1000Ω. The h-parameters are h_{ib} = 22Ω, h_{rb} = 3 x 10^{-4}, h_{fb} = - 0.98, h_{ob} = 0.5μA/V. Find current gain, voltage gain, input impedance and output impedance using approximate analysis.	[L3][CO6]	**[6M]**
	b)	Analyze CE amplifier with emitter resistance using simplified h-parameter model.	[L4][CO5]	**[6M]**
7	a)	Consider a single stage CE amplifier with R_s = 1kΩ, R_1 = 50kΩ, R_2 = 2kΩ, R_c = 1kΩ, R_L = 1.2kΩ, h_{fe}=50, h_{ie}=1.1k, h_{oe} = 25μA/V and h_{re}	[L4][CO5]	**[8M]**

		= 2.5 x 10^{-4}, as shown in Fig. Calculate A_I, R_i, A_v, A_{vs}, A_{IS} and R_0. 		
	b)	Differentiate between CE, CB and CC amplifiers.	[L2][CO5]	**[4M]**
8	a)	A CE amplifier is driven by a voltage source of internal resistance, Rs = 1000Ω and the load impedance of R_C=2kΩ. The h-parameters are h_{ie}=1.3k, h_{fe}=55, hoe = 22µA/V and h_{re} = 2 x10^{-4}. Neglecting biasing resistors, Estimate the value of current gain, voltage gain, input impedance, output impedance for the value of Emitter Resistor R_E = 200Ω inserted in the emitter circuit.	[L4][CO4]	**[8M]**
	b)	Draw the small signal model of FET.	[L1][CO2]	**[4M]**
9	a)	Define JFET parameters and establish relation between them.	[L1][CO2]	**[4M]**
	b)	Summarize the expressions for input impedance, output impedance and voltage gain of JFET Common Drain amplifier with neat diagram.	[L2][CO5]	**[8M]**
10	a)	For the circuit shown in figure below, determine input impedance, output impedance and voltage gain. 	[L3][CO5]	**[6M]**
	b)	Draw the circuit diagram of JFET Common Source amplifier with voltage divider bias for bypassed R_s and determine the expression for input impedance, output impedance and voltage gain.	[L3][CO5]	**[6M]**

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